WEB RESULTS by Google (Showing Results 21 - 30 of 7,340)

21. Stuck-Fault Tests **vs**. Actual Defects
... at normal V DD fail to operate at VLV; others operate at VLV, but at a reduced **speed**. ... Sam 1530 CUTs Figure 5. Venn diagram comparing VLV, normal V ...
crc.stanford.edu/crc_papers/ejmitc00a.pdf - 0 B

22. A High-**Speed** & High-Capacity Single-Chip Copper Crossbar
... as large as possible given the number of output interconnects required **vs**. ... Damiano et al.: **Speed** & High-Capacity Single-Chip Copper ... Cell **size** reductions ...
www.ece.ncsu.edu/erl/copper/cu_report.pdf - 0 B

23. LM2409 Monolithic Triple 9.5 ns CRT Driver
... by approximately 3% which corresponds to a **speed** degradation of ... driving an 8 pF load wi alternating ... Also, the length of the signal traces from the ...
pollux.dhcp.uia.mx/manuales/dos/display/LM2409.pdf - 0 B

24. LM2467 Monolithic Triple 7.5 ns CRT Driver
... This corresponds to a **speed** degrada- tion of 2% for every ... an 8 pF load with a 40 V pp alt Also, the length of the signal traces from the preamplifier ...
pollux.dhcp.uia.mx/manuales/dos/display/LM2467.pdf - 0 B

25. TECHNICAL INFORMATION
... is commonly called in the industry "V bump " and ... are small (20 pF), the **size** of the ... obta decoupling performance under high-**speed** transient conditions ...
www.powerdesigners.com/InfoWeb/design_center/Appnotes_Archive/dcplbsc.pdf - 0 B

26. Analysis of Packet Discarding Policies in High-**Speed** Networks
... 1 Introduction Many high **speed** networks applications generate messages ... dom variable th represents the length (number of ... Let V be the ran- dom variable that ...
www.ieee-infocom.org/1997/papers/sidi2.pdf - 0 B

27. Space and Water Heating Systems
... As for radiators Heat output **vs**. **size** and fan **speed** Internal fan Thermostat control of fan ... registers - direct supply of air to room **Size** Location ...
boris.uce.ac.uk/resources/LJ/ba203-SWHSystems.pdf - 0 B

28. TO BE RETURNED AT THE END OF THE EXAMINATION. THIS PAPER MUST NOT
... (b) A 7.5 kW, 250 V shunt motor ... Compute the full load **speed**. (20 marks) ... o . The air ga mm, stator bore radius r = 25 mm, and axial length l = 50 mm. ...
services.eng.uts.edu.au/~joe/subjects/eet/eet_fnlxm_a99_a.pdf - 0 B

29. Comparative Results for Verification
... corrected.In addition, the circuit and-**vs**-c illustrates ... sig-nals for verifying determinate **spe** independent **circuits**. ... are linear with respect the **size** of the ...
jungfrau.usc.edu/pub/iccad93.ps - 0 B

30. BUF634 250mA HIGH-**SPEED** BUFFER
... NOTES: (1) Tests are performed on high **speed** automatic test equipment ... Pad **Size** 4 x 4 0 Backing Chromium ... GAIN and PHASE **vs** FREQUENCY **vs** LOAD CAPACITANCE ...
www.uni-siegen.de/~holder/pdf/BUF634.pdf - 0 B

WEB RESULTS by Google (Showing Results 11 - 20 of 7,330)

11. Chapter 9. Principles of Electromechanical Energy Conversion
... the induced emf in an electrical circuit and force ... The diagram below shows a conductor of l placed ... B. When the conductor moves at a **speed** v, the induced ...
services.eng.uts.edu.au/~joe/subjects/ems/ems_ch9_nt.pdf - 0 B

12. CLC014 Adaptive Cable Equalizer for High **Speed** Data Recovery
... N August 1996 Comlinear CLC014Adaptive Cable Equalizer for High-**Speed** Data Recovery ... Cable Length ... Belden 8281 Cable Length (m) 500 400 100 0 50 250 ...
eshop.engineering.uiowa.edu/NI/pdfs/01/27/DS012726.pdf - 0 B

13. Petri Nets 2000
... with higher performance and smaller **size** • Performance of async **circuits** depends on: 1 ... t degree of concurrency (adds **speed**) **vs** control complexity ...
www.daimi.au.dk/pn2000/proceedings/pn2000_hardwareadd.pdf - 0 B

14. Circuit Media Choices Circuit Media Choices Twisted Pair Wire ...
... Speed' faster than Electricity on Copper 'Light Speed' faster than ... length installed 40% savi length installed **vs vs** copper copper ...
cpe.njit.edu/extnotes_ITV/MIS635/tec/TeamProject1.pdf - 0 B

15. PROMISE OF TUNNEL DIODE INTEGRATED **CIRCUITS**
... power, while numbers in parenthesis indicate a performance reduction, eg again in line 1, 3x access **speed** for the ... v ... 70 2009 Feature **Size** Production Year ...
www.nd.edu/~nano/downloads/991209SRCWorkshop.pdf - 0 B

16. DSL FAQ
... 4) Bottom Line, the ISDN **vs**. DSL choice comes down to use. ... A: The circuit **size** is depend bandwidth needs and desire for **speed**. ...
dsl.ibssnet.com/dsl_faq.html - 43 KB

17. Analog **vs**. Digital: A Comparison of Circuit Implementations for ...
... vm VDD(VDD - 2VT) 3(VDD– 3VT)+ (v.. - 5vT/2 ... digital circuit is more sensitive to changes Since changes in filter **size**, technology scaling, and operat ...
www.ee.rochester.edu:8080/users/friedman/papers/W1G03.pdf - 0 B

18. High-**Speed** Probing
... page 4 Figure 5. Probe input impedance **vs**. frequency. ... Shorter ground leads must be used making high-**speed** measurements. ... The small **size** of the lead ...
www.tek.com/Measurement/App_Notes/highspeedprobe/eng/55W_12107_0.pdf - 0 B

19. INTERNATIONAL RECTIFIER CORPORATION WARP **Speed**
... turn-on and turn-off switching performances when compared to two **size** larger Power ... the changes in the specs of the WARP **Speed** TM IGBTs ... Figure 4. IR **vs**. ...
www.irf.com/technical-info/whitepaper/wpwarp.pdf - 0 B

20. Microsoft PowerPoint - test_01_gsrc-6-00.ppt
... LFSR MISR Area # Test Fault **size size** overhead patterns Coverage ... Memory ËË At-**speed** No test overhead No test overhead ... V asr shu V asl shu ...
cadlab.ece.ucsb.edu/~soc/meetings/presentations/jun00/test_01_gsrc-6-00.pdf - 0 B

speed vs size circuits

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1. A Practical Repeater Insertion Method in High **Speed** VLSI **Circuits**
... A Practical Repeater Insertion Method in High **Speed** VLSI **Circuits** ... ratio of the transition t Elmore ... distance between repeaters, and the **size** of the ...
www.sigda.org/Archives/ProceedingArchives/Dac/Dac98/papers/1998/dac98/pdffi - 0 B

2. A Transmission Line Simulator for GaAs Integrated **Circuits**
... lines are presented in section 4. Run time results and **speed vs.** ... TABLE 1: STEP **SIZE VS.** provides a natural way of partitioning **circuits** into smaller ...
www.sigda.org/Archives/ProceedingArchives/Dac/Dac91/papers/1991/dac91/42_2/ - 26 KB

3. Measurement of simulation **speed**: its relation to simulation ...
... slowness" based on the total number and **size** of the ... be used to estimate what compromis **vs. speed** is desirable in a given neural circuit simulation ...
retina.anatomy.upenn.edu/~rob/cnschap.html - 13 KB

4. FPGA Routing Architecture: Segmentation and Buffering to Optimize ...
... 12000 14000 40 50 60 70 80 i ¢ £ ¤ ¥ Figure 4: **Speed** and area of FPGAs **vs.** routing wire s length. Critical path Routing area ...
www.eecg.toronto.edu/~vaughn/papers/fpga99a.pdf - 0 B

5. Circuit Design, Transistor Sizing and Wire Layout of FPGA ...
... pass transistor output voltage to 2.73V, which is ... delay, require more area for moderate **siz** and ... can signifi- cantly increase FPGA **speed** by increasing ...
www.eecg.toronto.edu/~vaughn/papers/cicc99.pdf - 0 B

6. Circuit Techniques for Low Power, High **Speed** Pipelined A/D
... pipeline, the **size** of the OpAmp is mainly determined by the sampling rate rather than the no constraint. ... **speed** of the OpAmp. ... GAP! Figure 3.6 Conductance **vs.** ...
kabuki.eecs.berkeley.edu/~gchien/thesis/Masters/ch3/chapter3.pdf - 0 B

7. Impact of Device Scaling on Analog Power Consumption
... The static current required to achieve the desired **speed** with a given capacitive ... 13 is that increases as the tran- sistor **size** W increases. ... Id **vs** Vgt ...
kabuki.eecs.berkeley.edu/~abo/papers/231/231_report.pdf - 0 B

8. Performance analysis of async **circuits** using Petri nets
... to construct **circuits** with higher performance and smaller **size.** Performance of async **circui** on ... degree of concurrency (adds **speed**) **vs** control complexity ...
www.lsi.upc.es/~jordic/gavina/BIB/files/atpn_tut5.ppt - 0 B

9. 9 Memory Devices & Chip Area
... 9/30/98 15 REVIEW Review x Memory technology selection involves tradeoffs • **Speed**+band **size** • Volatility/power/lifetime ...
www.ece.cmu.edu/~ece548/handouts/09device.pdf - 0 B

10. School of Physics--Academic: **Circuits**, DC **Circuits** and Components ...
... "Resistance" in **circuits** has a ... a conductor having a cross-sectional area A, a length L and ... for every atom in the conductor , (2) the **speed**, v, is the ...
www.physics.gatech.edu/academics/Classes/2k_summer/2212/a/circuits.html - 61 KB

WEB RESULTS by Google (Showing Results 21 - 30 of 12,100)

21. High-**Speed** Probing
... pulse ampli- tude is: 5 V - 0.005 V = 4.995 V Or, about ... page 4 Figure 5. Probe input imped ground leads must be used when making high-**speed** measurements ...
www.tek.com/Measurement/App_Notes/highspeedprobe/eng/55W_12107_0.pdf - 0 B

22. Accurate High **Speed** Empirically Based Predictive Modeling Of ...
... PODDAR AND BROOKE: ACCURATE HIGH **SPEED** EMPIRICALLY BASED PREDICTIVE ... The me **versus** optimized results for the test ... rectangular shape with a grid **size** of 9 ...
www.ee.duke.edu/~mbrooke/papers/1999/00746539.pdf - 0 B

23. A New RTD-FET Logic Family - Proceedings of the IEEE
... RTD as a function of the voltage V SUM when ... isolating them somewhat from the high-**spee** of ... challenging for **circuits** of even moderate **size** and, thus ...
dx.doi.org/10.1109%2F5.752517

24. DSL FAQ
... 4) Bottom Line, the ISDN vs. DSL choice comes down to use. ... A: The circuit **size** is depende bandwidth needs and desire for **speed**. ...
dsl.ibssnet.com/dsl_faq.html - 43 KB

25. Entry13
... to collect data which yield the horsepower and torque curves **versus** engine **speed**. ... A moc has not been constructed but might be the **size** of a 20 ...
www.rose-hulman.edu/~moloney/AppComp/2000Entries/Entry13/Entry13.htm - 9 KB

26. ENERGETICS OF BIPEDAL RUNNING
... E trans W b -1 was measured from the slope of the linear regression of energy cost against **s** Step length L c **versus** body weight. ...
spot.colorado.edu/~kram/bipeds.pdf - 0 B

27. A Genetic Algorithm For The High-Level Synthesis Of DSP Systems ...
... 3. Interconnect Capacitance **Versus** Area ... case the critical path has been halved, increasing of the ... The GA was executed with a population **size** of 750 ...
www.see.ed.ac.uk/~SLIg/papers/msb_3.pdf - 0 B

28. University of Waterloo Department of Electrical and Computer ...
... Efficiency.* **Speed versus** machine **size**. ... Equivalent circuit.* Tests: open-circuit and short Saturation.* Per-unit system.c. Special Transformers: ...
thunderbox.uwaterloo.ca/~claudio/courses/me269.ps - 0 B

29. untitled
... Storage **versus** Circuit **Size**. C. Chen, ICCAD '99 Embedded Tutorial, Session 12A. ... High-**Sp** Sizing Techniques based on Lagrangian Relaxation. Area vs. ...
www.engr.wisc.edu/ece/faculty/chen_charlie/iccad99ck.ppt - 0 B

30. Analysis of Packet Discarding Policies in High-**Speed** Networks
... 1 Introduction Many high **speed** networks applications generate messages ... dom variable th represents the length (number of ... Let V be the ran- dom variable that ...
www.ieee-infocom.org/1997/papers/sidi2.pdf - 0 B

WEB RESULTS by Google (Showing Results 11 - 20 of 12,100)

11. Performance analysis of async **circuits** using Petri nets
... Concurrency vs Complexity. ... Asynchronous **circuits**, whether **speed**-independent or with ti assumptions ... AP Boston-Dordrecht, 2000, part V, Architecture Modelling ...
www.lsi.upc.es/~jordic/gavina/BIB/files/atpn_tut5.ppt - 0 B

12. Impact of Device Scaling on Analog Power Consumption
... 2. I d vs Vgs , Vt for several channel lengths ... the device must be very large to achieve that **speed**. ... 3, which shows the optimum V gt **versus** L . The ...
kabuki.eecs.berkeley.edu/~abo/papers/231/231_report.pdf - 0 B

13. Design Considerations for High-**Speed** Low-Power Low-Voltage CMOS ...
... Noting that the stage requirements on the **speed** and accuracy become less ... Fig. 13 Power sampling frequency. ... 13 shows the measured power consumption vs. ...
kabuki.eecs.berkeley.edu/~tcho/Europaper.pdf - 0 B

14. 6Exam99
... (1). (h) In your answer book sketch an acceleration v. time graph ... (2). (e) Calculate the **siz** (2). Assume that the train maintains its **speed** of 8 ms -1 . ...
www.macleans.school.nz/students/science/physics/F6Exam98_99/6exam99.htm - 28 KB

15. Cryogenic Performance of a High-**Speed** GaInAs/InP pin Photodiode ...
... V. M ICROWAVE R ESPONSE The absolute response at room temperature was shown in ... tha 2) onto a superconducting high **speed** circuit chip (**size** of 5 ...
ieeexplore.ieee.org/iel1/50/12166/00557569.pdf

16. Modern Digital Design
... amplitude Page 38. Analog **versus** Digital (contd.) ... Lumped circuit assumption • Length of edge: t R t ... Page 46. High **speed** digital design Page 47. ...
cselab.snu.ac.kr/course/cad99/moderndigital.pdf - 0 B

17. Circuit Media Choices Circuit Media Choices Twisted Pair Wire ...
... Speed' faster than Electricity on Copper 'Light Speed' faster than ... length installed 40% savi length installed vs vs copper copper ...
cpe.njit.edu/extnotes_ITV/MIS635/tec/TeamProject1.pdf - 0 B

18. DSL FAQ
... 4) Bottom Line, the ISDN vs. DSL choice comes down to use. ... A: The circuit **size** is depende bandwidth needs and desire for **speed**. ...
dsl.ibssnet.com/dsl_faq.html - 43 KB

19. First Semester Examination June 1999 PHYSICS 1001 ENGN 1214 ...
... b Three identical uniform very thin rods of length, l, are ... The gure below shows two **circuits** ... the same **speed** v through the same uniform magnetic eld ...
www.anu.edu.au/Physics/courses/A01/phys1001_s1.pdf - 0 B

20. Transit Note #113 Specialization **versus** Configuration
Specialization **versus** Configuration. ... in an attempt to elicit the worst-case **size** and **speed** re ... are given, as well as the worst-case **size** and **speed** ...
www.cs.caltech.edu/research/ic/transit/tn113/tn113.html - 46 KB

WEB RESULTS by Google (Showing Results 1 - 10 of 12,100)

1. Measurement of simulation **speed**: its relation to simulation ...
... slowness" based on the total number and **size** of the ... be used to estimate what compromis vs. **speed** is desirable in a given neural circuit simulation ...
retina.anatomy.upenn.edu/~rob/cnschap.html - 13 KB

2. FPGA Routing Architecture: Segmentation and Buffering to Optimize ...
... 3.2 Delay Model Our delay values are all based on the delays in TSMC's 0.35 µm, 3.3 V CMOS Figure 4: **Speed** and area of FPGAs vs. ...
www.eecg.toronto.edu/~vaughn/papers/fpga99a.pdf - 0 B

3. Circuit Design, Transistor Sizing and Wire Layout of FPGA ...
... V W X Y ` a b c ... 7. Switch area - wire delay product vs. ... We again assume that routing wi out in metal 3. Table 1 lists the **speed** benefit from either ...
www.eecg.toronto.edu/~vaughn/papers/cicc99.pdf - 0 B

4. Distributed ESD protection for high-**speed** integrated **circuits** ...
... Page 2. KLEVELAND et al.: DISTRIBUTED ESD PROTECTION FOR HIGH-**SPEED** INTEGRATED 391 Fig. ... performance degradation **versus** line length for positive ...
haydn.stanford.edu/~bendik/pdf/edl_esd.pdf - 0 B

5. A Practical Repeater Insertion Method in High **Speed** VLSI **Circuits**
... T i V DD V DD V x – ---- In ... Practical Repeater Insertion Method in High **Speed** VLSI **Circui** the transition time vs the Elmore ...
www.sigda.org/Archives/ProceedingArchives/Dac/Dac98/papers/1998/dac98/pdffi - 0 B

6. A Transmission Line Simulator for GaAs Integrated **Circuits**
... related to the lossy lines are presented in section 4. Run time results and **speed** vs. ... for V d are 1.6 V and 0 V respectively. ... TABLE 1: STEP **SIZE** VS. ...
www.sigda.org/Archives/ProceedingArchives/Dac/Dac91/papers/1991/dac91/42_2/ - 26 KB

7. CMOS Current Amplifiers: **Speed versus** Nonlinearity
... CMOS Current Amplifiers: **Speed versus** Nonlinearity ... 16 2.1.1 Nonidealities due to the cha modulation . ... 5 System aspects of current-mode **circuits** 127 ...
lib.hut.fi/Diss/2000/isbn9512252139/isbn9512252139.pdf - 0 B

8. INTERNATIONAL RECTIFIER CORPORATION WARP **Speed**
... turn-off switching performances when compared to two **size** larger Power ... Figure 4. IR vs. compares the costs of the WARP **Speed versus** alternatives below ...
www.irf.com/technical-info/whitepaper/wpwarp.pdf - 0 B

9. Impact of Device Scaling on Analog Power Consumption
... 2. I d vs Vgs , Vt for several channel lengths ... the device must be very large to achieve that **speed**. ... 3, which shows the optimum V gt **versus** L . The ...
kabuki.eecs.berkeley.edu/~abo/papers/231/231_report.pdf - 0 B

10. Performance analysis of async **circuits** using Petri nets
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www.lsi.upc.es/~jordic/gavina/BIB/files/atpn_tut5.ppt - 0 B

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1. Measurement of simulation **speed**: its relation to simulation ...
... slowness" based on the total number and **size** of the ... be used to estimate what compromis vs. **speed** is desirable in a given neural **circuit** simulation ...
retina.anatomy.upenn.edu/~rob/cnschap.html - 13 KB

2. **Circuit** Design, Transistor Sizing and Wire Layout of FPGA ...
... length (ie the delay to pass one logic block) **versus** the **size** of ... Thus some of the **speed** ga buffer's increased ... 6. Delay per logic block spanned vs. ...
www.eecg.toronto.edu/~vaughn/papers/cicc99.pdf - 0 B

3. FPGA Routing Architecture: Segmentation and Buffering to Optimize ...
... in TSMC's 0.35 µm, 3.3 V CMOS process ... by pass transistors, has extremely poor **speed** — 2: Best buffered, two different length architectures vs. ...
www.eecg.toronto.edu/~vaughn/papers/fpga99a.pdf - 0 B

4. Disk Partitioning on VMS: What, Why, When and How
... Bridges; Cut-through (a la GIGAswitch) vs. ... Can't get around the **speed** of light and its late over long distances; ... Local **versus** Remote operations. ...
www.geocities.com/keithparris/decus_presentations/s99_long_distance.ppt - 0 B

5. **Circuit** Media Choices **Circuit** Media Choices Twisted Pair Wire ...
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cpe.njit.edu/extnotes_ITV/MIS635/tec/TeamProject1.pdf - 0 B

6. Entry13
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www.rose-hulman.edu/~moloney/AppComp/2000Entries/Entry13/Entry13.htm - 9 KB

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lib.hut.fi/Diss/2000/isbn9512252139/isbn9512252139.pdf - 0 B

8. 6Exam99
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www.macleans.school.nz/students/science/physics/F6Exam98_99/6exam99.htm - 28 KB

9. INTERNATIONAL RECTIFIER CORPORATION WARP **Speed**
... turn-off switching performances when compared to two **size** larger Power ... Figure 4. IR vs. compares the costs of the WARP **Speed versus** alternatives below ...
www.irf.com/technical-info/whitepaper/wpwarp.pdf - 0 B

10. Dynamic Logic and Latches II:
... Die **Size** 16.5 mm x 18.1 mm ... 0.35 process 9.66 Million 14.4 mm x 14.5 mm 3.3V external internal 25W @ 433 MHz 433 MHz ... I Required to function at 1/10th **speed** ...
www.stanford.edu/class/ee371/handouts/gronowski96.pdf - 0 B

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1. Scalable Functional Self-Test Methodologies for Component- Based ...
... At-**speed** testing of ... Cycle2 V 2 V 3 101 Transition F or R C CCR ... 10 Functionally True Pat **Size** Functionally True Paths and Fault **Size ALU** AC **ALU** ...
cadlab.ece.ucsb.edu/~soc/meetings/presentations/sep99_24/tim/soc_sep99.pdf - 0 B

2. Microsoft PowerPoint - test_01_gsrc-6-00.ppt
... LFSR MISR Area # Test Fault **size size** overhead patterns Coverage ... Memory ËË At-**speed** No test overhead No test overhead ... V asr shu V asl shu ...
cadlab.ece.ucsb.edu/~soc/meetings/presentations/jun00/test_01_gsrc-6-00.pdf - 0 B

3. Xtensa A new ISA and Approach
... Target specifications • eg synthesize for area at the cost of **speed** ... 24 Early Controversies Performance/scalability **vs.** code **size** Performance/scalability **vs.** ...
bwrc.eecs.berkeley.edu/Classes/CS252/Notes/xtensa_022400.pdf - 0 B

4. 10 Multi-Level Strategies
... Increases throughput • Up to 3x improvement in clock **speed** if cache ... x Tradeoff for large **vs.** ... 2 @ 32 bits data / clock • L1 Block **Size** = 256 bits ...
www.ece.cmu.edu/~ece548/handouts/10levels.pdf - 0 B

5. Stack Computers: CONTENTS
... non-register machines; 6.1.2 High level language **vs.** ... DIFFERENCES FROM CONVENTIONAL 6.2.1 Program **size**; ... 6.3.3.1 Execution **speed** gains; 6.3.3.2 Memory **size** ...
www.ece.cmu.edu/~koopman/stack_computers/contents.html - 17 KB

6. MICROPROCESSORS
... processes use bipolar transistors for increased **speed** and CMOS ... Feasible (good) choices **v** (supported) (3) Instruction Format (length, **size** of various ...
www.davv.ac.in/onlinelectures/21CPU.htm - 75 KB

7. Asynchronous VLSI System Design Takashi Nanya Research Center for ...
... **Speed**-Independent: Unbounded gate delays with no wire delays Delay ... Fabricated in NEC's V CMOS Process with 3 ... Die **size**: 12 : 15 mm 12 : 15 mm ...
www.hal.rcast.u-tokyo.ac.jp/titac2/Nanya-ASP-DAC98.pdf - 0 B

8. What is CISC technology
CISC **vs** RISC Technology. ... space, individual instructions could be of almost any length - this m memory **speed** increased, and high-level languages displaced ...
www.sunderland.ac.uk/~ts0jti/comparch/ciscrisc.htm - 14 KB

9. Lecture 5: Vector Processors and DSPs
... of the impact of start-up • N V : The vector length needed to make vector mode faster than s - measures both start-up and **speed** of scalars ...
american.cs.ucdavis.edu/academic/ecs201a/fred/l5.pdf - 0 B

10. Designing the Low-Power M • CORE Architecture
... 4.1.1 Synthesizable **vs.** ... In each step, Focus picks a set of candidate transistors to **size** bas sensitiv- ity to the ... Figure 2: **Speed** and area trade-off ...
www.ece.umd.edu/courses/enee759m.S2000/papers/scott1998-lowpower.pdf - 0 B

WEB RESULTS by Google (Showing Results 1 - 10 of 596)

1. A Transmission Line Simulator for GaAs Integrated Circuits
... lossy lines are presented in section 4. Run time results and **speed vs.** ... TABLE 1: STEP **SIZE** machine) for simulating a 16 bit ripple carry **adder** with varying ...
www.sigda.org/Archives/ProceedingArchives/Dac/Dac91/papers/1991/dac91/42_2/ - 26 KB

2. High-**Speed** MARS Hardware
... High-**speed** MARS encryption/decryption hardware was developed ... design is the special **ad** multiplier. ... Finally, performance and **size** estimates are presented ...
www.research.ibm.com/security/aes3.pdf - 0 B

3. Scaling Accumulator Multipliers
... implement this operation in HW that has the traditional trade off **size vs. speed.** ... This solu the **size** "eliminates" the multiplier and performs the ...
www.geocities.com/SiliconValley/Pines/6639/ip/scal_mac.html - 6 KB

4. Reconfigurable Hardware Testbed for Digital Signal Processing
... FPGA **vs.** DSP ? **Speed • Speed** of FPGA 10x **speed** of DSP Note: ... Page 6. FPGA **vs.** DSP ? parallelism ... Algorithm Inputtype **Size** (#slice) SynthesisTime ...
bwrc.eecs.berkeley.edu/Presentations/Retreats/Winter_Retreat_Jan_2000/Poste - 0 B

5. Energy-Delay Estimation Technique for High-Performance ...
... estimation of various VLSI adders using Logical Effort **vs.** ... sizes (all optimal in terms of **spe** determined by ... obtained when using the same input **size** for each ...
www.dec.usc.es/arith16/papers/paper-193.pdf - 0 B

6. Low-Power, Low-Noise **Adder** Design with Pass-transistor Adiabatic ...
... All device sizes are minimum **size** in a 0.6-µm CMOS technology. ... Standard cells were optim power and high **speed.** ... 6. Energy consumption **vs.** frequency ...
min.ecn.purdue.edu/~mahmoodi/icm00.pdf - 0 B

7. Performance analysis of async circuits using Petri nets
... Important tradeoff: degree of concurrency (adds **speed**) **vs** control complexity (reduces **spe** increases **size**). ... Concurrency **vs** Complexity. req1+. start+. ...
www.lsi.upc.es/~jordic/gavina/BIB/files/atpn_tut5.ppt - 0 B

8. 1. Description of Omnilab Equipment and Interconnection
... in three tests performed and in the sample **size** of 5 ... **speed** (1.5MHz) to highest clock **spee** by ... 6. Comparison Results with Irsim Results: Simulation **Vs.** ...
www-ece.rice.edu/Courses/422/1997/hkim/elec423.pdf - 0 B

9. Designing the Low-Power M • CORE Architecture
... one instruction (FF1), a hardware loop instruction (LOOPT), and instructions to **speed** up me 16-Bit **vs.** ... In addition, a die **size** of just over 2 mm 2 was ...
www.ece.umd.edu/courses/enee759m.S2000/papers/scott1998-lowpower.pdf - 0 B

10. Efficiency of Adiabatic Logic for Low-Power, Low-Noise VLSI
... All device sizes are minimum **size** in a 0.6-µm CMOS technology. ... logic is more efficient for where the **speed** of operation ... 6. Energy consumption **vs.** ...
www.utdallas.edu/~nourani/Research/papers/mwscas00.pdf - 0 B

WEB RESULTS by Google (Showing Results 11 - 20 of 596)

11. A 14-bit, 5-MHz Digital-to-Analog Converter Using Multi-bit S ...
... The **size** of the adders in these blocks were chosen to meet the **speed** requirements for simp Measured SNR and SNDR **vs**. signal magnitude. Fig. ...
cis.stanford.edu/icl/wooley-grp/katayoun/VLSI_paper.pdf - 0 B

12. Gallium Arsenide Process Evaluation Based on a RISC
... Fig. 10: : SRAM cell power **vs**. cell **size** for three load devices: a normal depletion load, a spe depletion load having a more ... device switching **speed**. ...
www.eecs.umich.edu/UMichMP/Publications/12-93.ps - 0 B

13. Knowledge Base • A knowledge base is a set of representations of ...
... 2.Decide on a vocabulary of predicates, functions, and constants • **size** as a function or predi **vs** bigness; small as relative **size** or ... **size**? ... **speed**? ...
www.engr.uvic.ca/~aschoorl/ceng420/notes/Knowledge_Engineering.pdf - 0 B

14. Performance Tradeoffs in Digit-Serial DSP Systems
... 3 Digit-serial Programmable DSP **vs**. ... such as video image processing and high **speed** comm dedicated ... The digit-**size** of the digit-serial units is 4 and ...
www.ece.umn.edu/groups/ddp/Publications/suzuki/ds_paper_asilo.ps - 0 B

15. Petri Nets 2000
... be applied • Important tradeoff: degree of concurrency (adds **speed**) **vs** control complexity (**speed** and increases **size**) ... Concurrency **vs** Complexity ...
www.daimi.au.dk/pn2000/proceedings/pn2000_hardwareadd.pdf - 0 B

16. Hybrid Signed Digit Representation for Low Power Arithmetic ...
... whereas the delay of the HSD-1 **adder** is about 6 gates [9], irrespective of the word length. further power reduction at the expense of **speed**. ...
www.csee.umbc.edu/~phatak/publications/hsd-lowpower.pdf - 0 B

17. Microsoft PowerPoint - Lec07-vector
... of the impact of start-up • N V : The vector length needed to make vector mode faster than s - measures both start-up and **speed** of scalars ...
bwrc.eecs.berkeley.edu/Classes/CS252/Notes/Lec07_vector.pdf - 0 B

18. THÈSE
... v ... count on chips, the push for higher **speed** and lower power makes it ... ers architectures to the **size**, critical path length, wiring complexity and ...
tima.imag.fr/publications/files/th/mao_81.pdf

19. Parallel Sequence Comparison and Alignment
... Figure 2. Seconds **vs**. length for search and alignment of proteins (affine or BLAST). ... Progra processors attempt to mix the **speed** of single-purpose ...
www.cse.ucsc.edu/research/kestrel/papers/asap95.pdf - 0 B

20. semi98 slides
... mwe/IFF/14. Single-ended **vs**. Double-ended. Any function of inputs. ... 1. 1. Select. mwe/IFF Tree High-**speed** Output. 2 x 165 ps. mwe/IFF/21. ... Carry. Type. 32 ...
inp.cie.rpi.edu/research/mcdonald/frisc/students/mernest/slides/IFF.ppt - 0 B

WEB RESULTS by Google (Showing Results 11 - 20 of 596)

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www.eecs.umich.edu/UMichMP/Publications/12-93.ps - 0 B

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www.ece.umn.edu/groups/ddp/Publications/suzuki/ds_paper_asilo.ps - 0 B

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www.daimi.au.dk/pn2000/proceedings/pn2000_hardwareadd.pdf - 0 B

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www.csee.umbc.edu/~phatak/publications/hsd-lowpower.pdf - 0 B

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bwrc.eecs.berkeley.edu/Classes/CS252/Notes/Lec07_vector.pdf - 0 B

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tima.imag.fr/publications/files/th/mao_81.pdf

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www.cse.ucsc.edu/research/kestrel/papers/asap95.pdf - 0 B

20. semi98 slides
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inp.cie.rpi.edu/research/mcdonald/frisc/students/mernest/slides/IFF.ppt - 0 B

WEB RESULTS by Google (Showing Results 1 - 10 of 666)

1. Suggestions for Exercises
... **serial adder**/subtracter: mode **input** '0' = add, '1' = subtract; ... waveform, phase durations inputs or register ... **multi**-tap delay line: fixed delay, or ...
www.ashenden.com.au/designers-guide/DG-exercise-suggestions.html - 9 KB

2. Xilinx XCell 20 Article: Distributed Arithmetic Laplacian Filter ...
... 1 **input** is used as the carry **input** to the ... LUT plus 18 **serial** adders and one 9-bit **parallel** With the **multi**- plier-accumulator reduced to such a small size ...
www.xilinx.com/xcell/xl20/xl20-38.pdf - 0 B

3. A Firmlib k"nyvt r cell inak list ja (a Process-Independent ...
... n) es2add2 2-bit full **adder** es2and Multiple ... NOR es2ntri Tristate butfer es2or Multiple-**inpu** es2reg4 ... controls) es2sreg ps Shift register (**parallel** in, **serial** ...
www.eet.bme.hu/~poppe/solotex/lib_firm.txt - 5 KB

4. Bin Xu and Farhan Rana: 6.371 Project
... TIMING CONTROL FOR **MULTI-INPUT** OUTPUT CIRCUITS : ... Dual-rail three inputs xor3 gate gate ... for each individual component including **adder**, shift registers ...
6371.lcs.mit.edu/Fall96/reports/xu_rana/project.html - 14 KB

5. Lecture 8 Multioperand Addition Uses of Multioperand Addition
... Counts the number of 1's among the n inputs ... 4-bit binary full **adder**, with carry in, is a (2, counter Page 13. ... Adding Multiple Signed Numbers ...
www.ee.byu.edu/ee/class/ee621/Lectures/L08.PDF - 0 B

6. National CD-ROM Alphanumeric Listing
... with TRI-STATE Outputs 54F258A Quad 2-**Input** Multiplexer with ... Checker 54F283 4-Bit Bin **Adder** with Fast ... Shift/Storage Register with Common **Parallel** I/O ...
eshop.engineering.uiowa.edu/NI/DISK1ALN.PDF - 0 B

7. WEEK 1:
... Full **adder** as full subtractor; Number Systems; Sign ... using T; Invalid states, invalid **input** Timing ... **Multi**-phase Clocks; Simple examples; Effect of clock ...
www-cad.eecs.berkeley.edu/~newton/Classes/CS150sp97/lecture.htm - 19 KB

8. VLSI Circuit Design - I
... **Multi-input** gates and complex gates; Optimization of logic ... area comparison of various **ad** ... **Serial** multiplier; **Serial-parallel** multiplier; **Parallel** array ...
ece.wpi.edu/~leblebic/epfl_vlsi.htm - 6 KB

9. An Efficient **Parallel Adder** Based Design for One Dimensional ...
... The multiplication of an **input** operand by a sine or ... a CORDIC pro- cessor operated serially cycles. ... An Efficient **Parallel Adder** Based Design for One ...
nr.stic.gov.tw/ejournal/ProceedingA/v24n3/195-204.pdf - 0 B

10. CmpSci 535 Lecture 5
... The **adder** operates in constant time, but it takes a ... the bits of the register together using m **input** lines but ... of this signal with the clock **input** to the ...
www.cs.umass.edu/~weems/CmpSci535/535lecture5.html - 21 KB

WEB RESULTS by Google (Showing Results 11 - 20 of 666)

11. Design and FPGA implementation of Digit-**Serial** FIR filters
... cell is fed to the least significant full **adder** of the ... 4.2.- Multiple precision to single precision Fig.8. Format 3 to 1 block: a) digit **input** sequence; b ...
www.ii.uam.es/~ivan/icecs98-fir.pdf - 0 B

12. FPGA-based FIR Filter Using Bit-**Serial** Digital Signal Processing
... This **adder** tree has three levels of bit-**serial** adders and ... rations" in VHDL, based upon the parameters ... ap-proaches have been extended to **multi**-FPGA systems ...
www.tecnun.com/asignaturas/tratamiento%20digital/use-bitserial.ps - 0 B

13. Digital Filters in AT6000 FPGAs - Application Note
... the upper limit to these kinds of **multi**-chip systems ... multipliers and a **serial** column **adder** ... This multiplier has one **serial input**, one **parallel input** ...
www.tecnun.com/asignaturas/tratamiento%20digital/imp-bitserial.pdf - 0 B

14. FPGA-BASED FIR FILTERS USING DIGIT-**SERIAL** ARITHMETIC
... Digit-**serial adder** ... Type of 4-**input** 3-**input** Flip- Speed FIR filters LUTs LUTs flops ... and W "High-level bitserial datapath synthesis for **multi**-FPGA systems ...
www.ece.umn.edu/groups/ddp/Publications/hhlee/hhlee.ps - 0 B

15. MorphoSys : An Integrated Reconfigurable System for Data-**Parallel** ...
... **Multi**-context systems may be dynamically reconfigurable ... 4). The fourth port takes **input** output register ... The ALU **adder** is 28 bits wide to prevent loss of ...
www.eng.uci.edu/morphosys/docs/sbcci98.html - 35 KB

16. StReAm: Object-Oriented Programming of Stream Architectures using ...
... FIFO buffer **Adder** Counter Register ... the **input** variables. In addition, the rotate function de a **multi-input, multi**-output module instantiation by ...
www.doc.ic.ac.uk/~oskar/pubs/fpl00.ps - 0 B

17. StReAm: Object-Oriented Programming of Stream Architectures using ...
... PaModules may consist of multiple PamBlox and are op- timized for a ... FIFO buffer **Adder** Co Register ... IDEA round can be mapped to a four-**input**, four- output ...
www.doc.ic.ac.uk/~oskar/pubs/fpl00.pdf - 0 B

18. Design and Low Speed Testing of a Four-Bit RSFQ Multiplier ...
... a simpleaddition of bits from a **serial input**; and thus ... bit words, as compared to multiple multiplications withaccumulation ... The use of an **adder**-accumulator, as ...
www.ece.rochester.edu/~sde/research/publications/asc96/lowspeed.ps - 0 B

19. Performance/Power Tradeos in ASIC Multipliers 1 Introduction
... it does not require the generation of the hard multiple with a ... is slower due to the nal ripple Booth ... very well since a switch at an **input** pin always ...
www.dice.ucl.ac.be/~anmarie/patmos/papers/S2/2_2.pdf - 0 B

20. A Multiplier with Redundant Operands
... are not at all uniform, since some of the inputs come from ... HA: Half **Adder**, FA: Full **Adder** in the design of the multiplier, a program, **multi**- gen, was ...
arith.cs.ucla.edu/publications/ferguson_asilomar99.pdf - 0 B

WEB RESULTS by Google (Showing Results 1 - 10 of 1,030)

1. Digital Switching Overview
... Use a **multiple** function ALU. Store the program steps as binary operation codes in random a memory (RAM). ... Page 76. **Parallel vs. Serial**. ...
engr.smu.edu/~levine/ee8302/digintro.ppt - 0 B

2. Gord Allan
... in 2 places - Full case **vs Parallel** Case - case ... in verilog - assign **vs** structural **vs** always bl complement* Auxilliary notes on bit-**serial adder**, CSA **adder** ...
web.doe.carleton.ca/~gallan/478/ - 22 KB

3. EXPERIMENT 8
... Digital electronics carry information as a series of pulses on a single line (**serial**) or on severa simultaneously (**parallel**). ... Signal Output **vs**. ...
www.chem.unc.edu/undergrads/2002fall/chem142l_wightman/experiments/EXPERIME - 0 B

4. VHDL samples
... The VHDL source code for a **serial** divider, using a shortcut model where a signal ... Example 4-bit divider model. ... Simple example of component **vs** entity. ...
www.csee.umbc.edu/help/VHDL/samples/samples.shtml - 16 KB

5. Digital Device Components
... ported access. Or by their data retention characteristics: Dynamic **vs**. ... **Serial** addition can b area is a ... Compute the carries to each stage in **parallel**. ...
www.csee.umbc.edu/~plusquel/vlsi/slides/chap8_1.html - 31 KB

6. Microsoft PowerPoint - lecture5
... 15 • Amount of parallelism in application may be limited • Extra capacitance overhead of **mu** datapaths ... 20 **Serial vs. Parallel Adder** Power ...
www.ece.ucdavis.edu/~ramirtha/EEC289O/lecture5.pdf - 0 B

7. Microsoft PowerPoint - eea051-06.ppt
... how many times the registers are shifted • **serial vs**. ... 4-bit register, register with **parallel serial adder**, second-form **serial adder**, universal shift ...
www2.nuk.edu.tw/dpcs/teacher/wuch/eea051/eea051-06.pdf - 0 B

8. Chapter 5 Arithmetic and Logical Operations
... 1. 0. C. B. Note: **Parallel** structure on top, **serial** on bottom. Logic Gates. CMPE12c. Cyrus B Cyrus Bazeghi. Combinational **vs**. Sequential. Combinational Circuit ...
www.soe.ucsc.edu/classes/cmpe012c/Summer04/notes/Digital_Logic_9.ppt - 0 B

9. WEEK 1:
... RAMs, ROMs; Registers as memory; **serial** & **parallel**; Magnetic and optical memories; Rand memory: SRAM, DRAM; ... Completely **vs**. ...
www-cad.eecs.berkeley.edu/~newton/Classes/CS150sp97/lecture.htm - 19 KB

10. **Parallel multiple**-symbol variable-length decoding - Computer ...
... different from [3, 6, 8]). It de- codes **multiple** symbols (different ... Figure 3. Register size **v** 4. Organization of **parallel/serial** code- word detection. ...
ce.et.tudelft.nl/publicationfiles/656_389_01106759.pdf - 0 B